SEMICONDUCTOR WAFERS HAVING ASYMMETRIC EDGE PROFILES THAT FACILITATE HIGH YIELD PROCESSING BY INHIBITING PARTICULATE CONTAMINATION AND METHODS OF FORMING SAME

Abstract of the Disclosure

Semiconductor wafers utilize asymmetric edge profiles (EP) to facilitate higher yield semiconductor device processing. These edge profiles are configured to reduce the volume of thin film residues that may form on a top surface of a semiconductor wafer at locations adjacent a peripheral edge thereof. These edges profiles are also configured to inhibit redeposition of residue particulates on the top surfaces of the wafers during semiconductor processing steps. Such steps may include surface cleaning and rinsing steps that may include passing a cleaning or rinsing solution across a wafer or batch of wafers that are held by a cartridge and submerged in the solution.

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